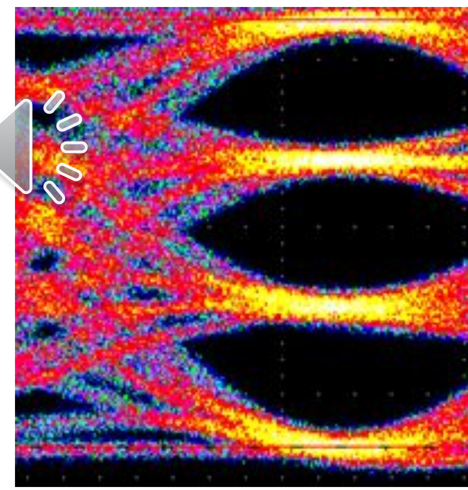
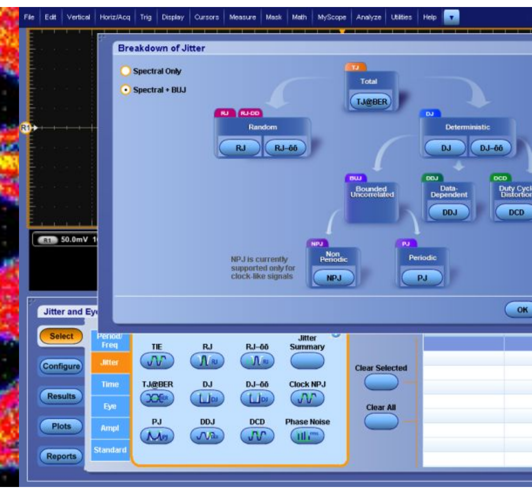
Verifying NRZ and PAM4 Performance in 28G & 56G Designs





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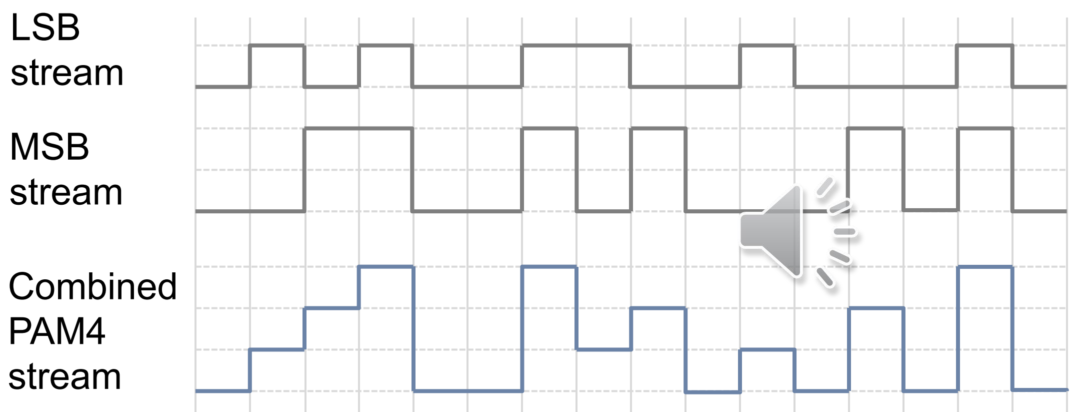
November 4, 2014

Agenda

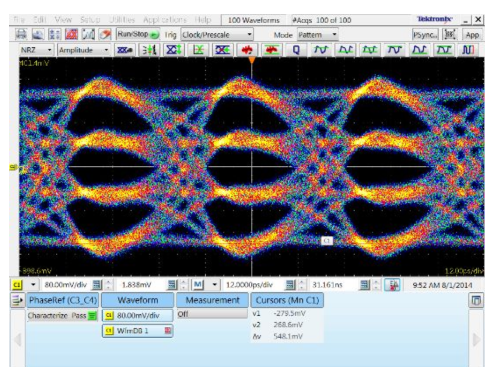
- PAM Technology Overview
  - PAM vs NRZ methods of communication
  - Where PAM fits in the standards community
  - Challenges with PAM signaling
- Recommended methods for validating PAM signaling
  - Transmitter Test
    - Oscilloscope-based Analysis tools
  - Receiver Test
    - Signal Generation and Error Detection tools
- Q&A/Resources for you

What is PAM?

- **P**ulse **A**mplitude **M**odulation
  - PAM4 combines two bit streams and uses 4 levels to encode 2 bits into 1 UI
  - For Example, 56 Gbit/s PAM4 runs at a symbol rate of 28 GBaud

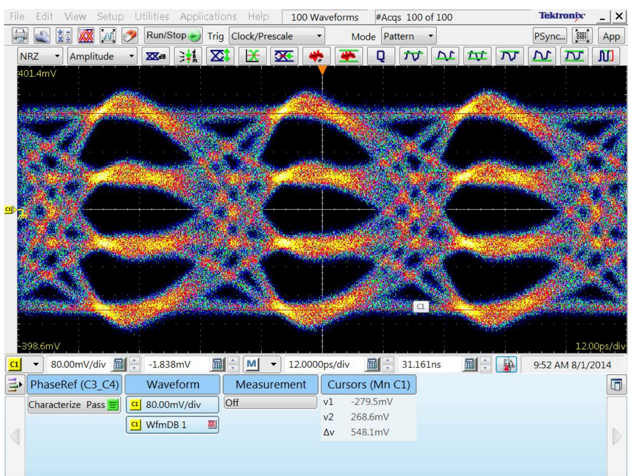


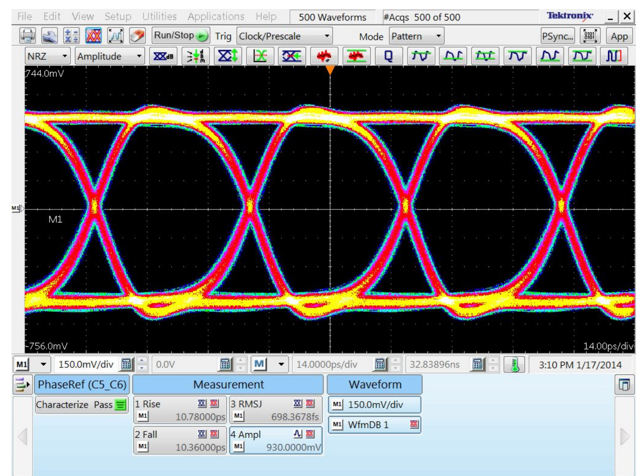
MSB	LSB	PAM4 LEVEL
0	0	0
0	1	1
1	0	2
1	1	3



What are the differences between PAM4 and NRZ?

- PAM4
  - 4 Levels -> 3 Eyes
  - Sensitive to SNR (eyes smaller)
  - 2 bits into 1 UI
  - ½ Baud Rate for same data throughput (28 GBaud = 56Gbps)
  - Adds complexity/cost to Tx/Rx
- NRZ
  - 2 Levels -> 1 Eye
  - Less Sensitive to SNR
  - 1 bit in 1 UI
  - 2X Baud Rate for same data throughput (28GBaud = 28Gbps)
  - Less expensive Tx/Rx





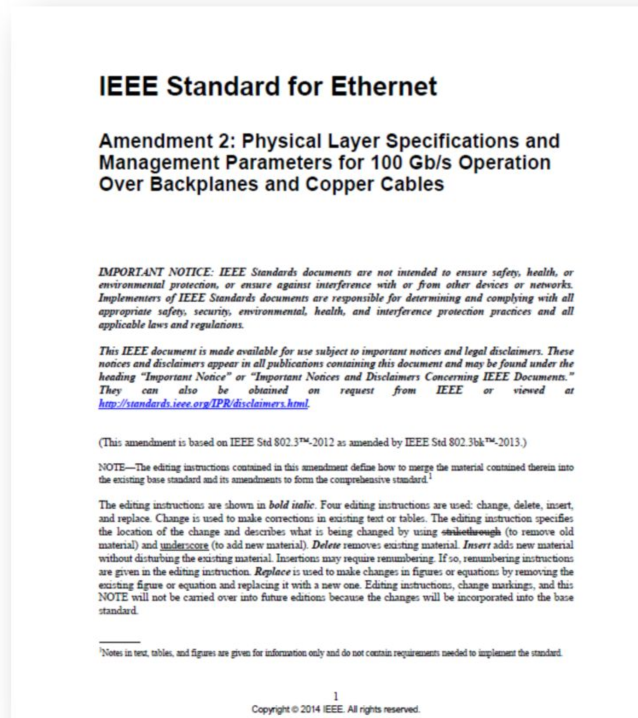
200G/400G Market Situation

- Current NRZ designs (25GBd) have two options for increasing throughput
  - 56 GBd NRZ
    - Targeted toward supporting a broad set of reach objectives ranging from die to die (10mm USR), chip to optical engine (50mm XSR), chip to pluggable module (100mm VSR) and chip to chip (500mm MR).
  - 28 GBd PAM4, with early discussions of 56 GBd PAM4
    - Extend beyond 3” channels

CEI-56G Project	Application	Loss dB	Max Reach mm
Ultra Short Reach USR	Chip-to-OE (within MCM)	not stated	10
Extra Short Reach XSR	Chip-to-OE (Chip-to-PHY)	5 to 10 @ 28G	50
Very Short Reach VSR	Chip-to-Module	10 to 20 @ 28G	100
Medium Reach MR	Chip-to-Chip	15 to 25 @14G	500
Long Reach LR (not a project)	*Backplane (Chip-to-Fabric)*	*25 to 50 @ 14G*	*1000*

Next Generation Standards Update

- IEEE802.3bj
  - PAM4 (100GBASE-KP4 4x 13.8GBd) is defined in the IEEE 802.3bj
  - Goal was to leverage legacy backplanes, however re-designed backplanes using NRZ (100GBASE-KR4 4x 25.78 GBd) was widely adopted
- OIF CEI 4.0 Draft Specification
  - 56GBd NRZ for USR applications
  - 28GBd PAM4 for CEI-56G-LR



IEEE Standard for Ethernet

Amendment 2: Physical Layer Specifications and Management Parameters for 100 Gb/s Operation Over Backplanes and Copper Cables

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(This amendment is based on IEEE Std 802.3™-2012 as amended by IEEE Std 802.3bk™-2013.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.[1]

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. Change is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

[1]Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1

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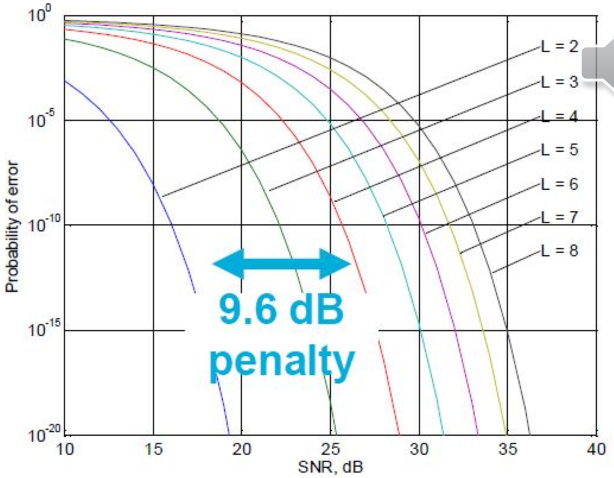
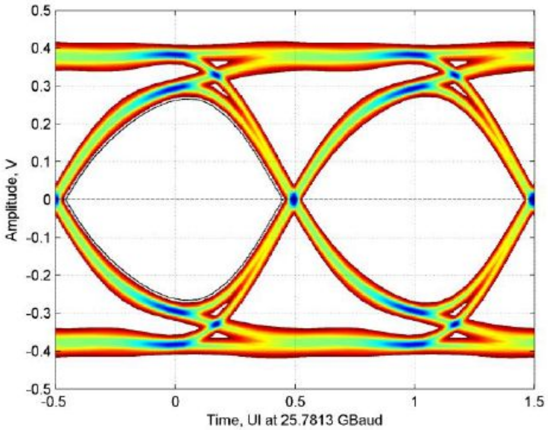
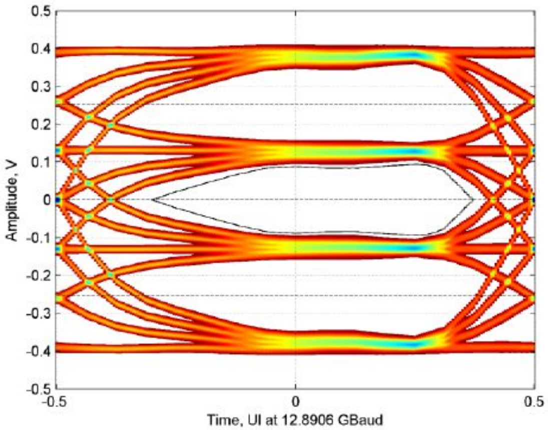
PAM Signaling Challenges

- Multiple bits/symbols → reduce symbol rate
- Level separation loss must be offset by…
  - Reduction in channel loss
  - More powerful equalization
  - Forward Error Correction



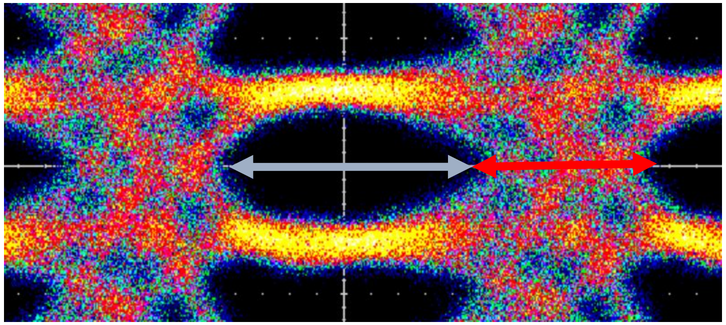




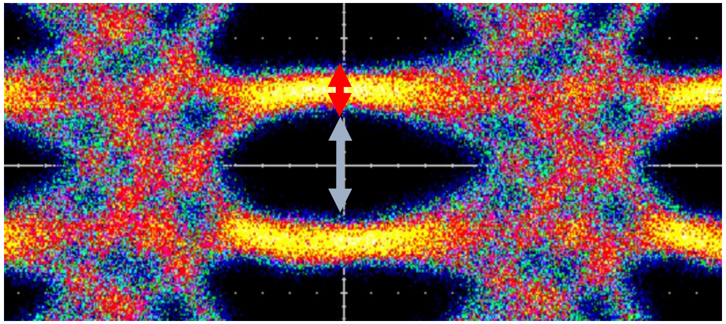
Improve bandwidth efficiency at the expense of complexity.

PAM4 Measurement Challenges

- What do measurements on individual eyes mean relative to overall link BER
- Extend Noise and Jitter decomposition concepts to PAM4
  - For example, what does a BER contour mean on 3 eyes relative to the overall link
- Troubleshoot and understand the effects of ISI due to multiple transitions
- Concept of aggregate measurements – linearity, noise, etc.



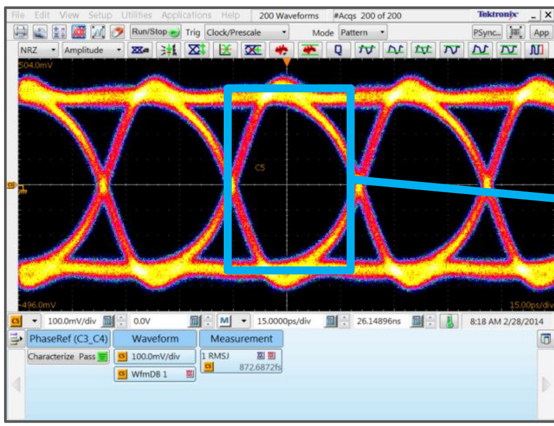
Horizontal PAM4 signal measurement

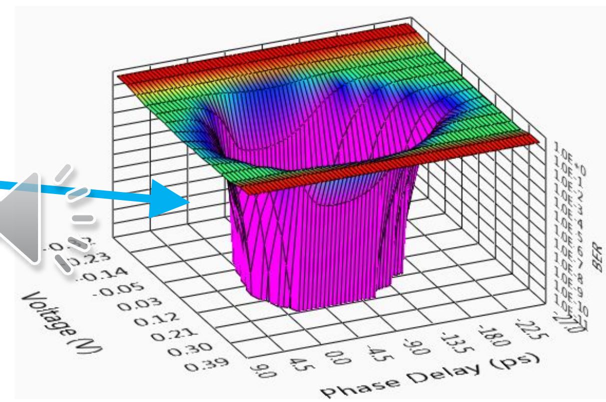


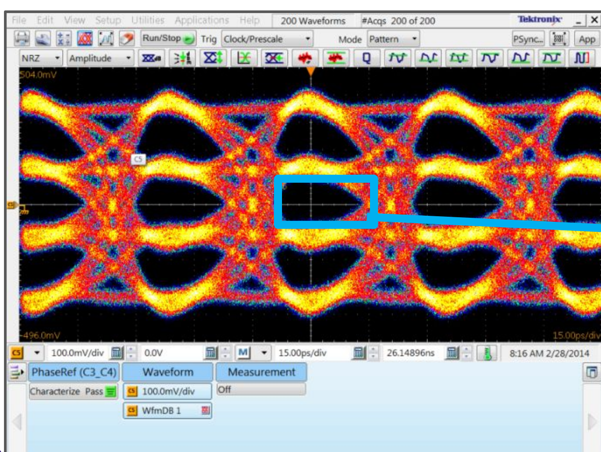
Vertical PAM4 signal measurement

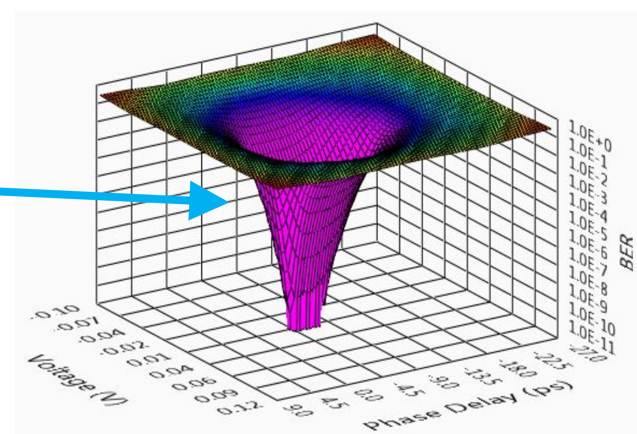
PAM4 Measurement Challenges

- PAM4 BER measurement methodologies?
  - Contour plot opening reduced PAM4 (vs NRZ) due to added deterministic jitter/noise
  - Industry specs moving to ~1E-5 BER for PAM4, as opposed to 1E-12/1E-15 for NRZ
  - Low BER measurements are critical to ensure detection of low-probability events/floors









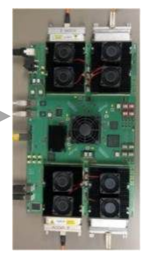
Test Methodologies for PAM Signaling Validation

Signal Generation

- **Fast enough signal rise time?**
- **Deep Pattern Length (PRBS)?**
- **Flexible pattern definition?**
    - **Jitter**
    - **Amplitude**

Test Signal

Device Under Test
Transceiver chipset,
Gearbox



Signal Acquisition

- **Optical & Electrical Signals?**
- **Adequate Dynamic Range?**
- **Event Capture/Trigger?**
- **Measurement system B/W?**

Analysis Software

- **Threshold/level detection?**
- **Render a multi-level eye?**
- **Provide jitter & noise results?**
- **Make a BER measurement?**
- **Compare to spec reference?**

Build a test strategy that works with your measurement task

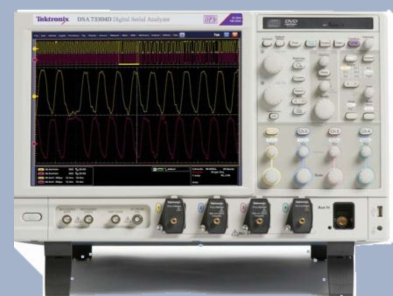
Considerations for a PAM4 Signal Acquisition System

System

Add-In Cards

Chip

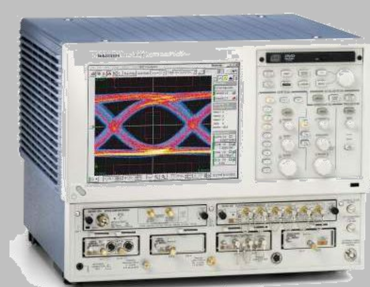
R&D | Verification/Compliance | Manufacturing



Real-time Scopes

The most versatile tool for all areas of high-speed digital and analog applications

- ✓ Single shot acquisition ideal for post processing
- ✓ Most advanced trigger system to identify unique events
- ✓ Most flexible software-based clock recovery
- ✓ Debugging and Troubleshooting



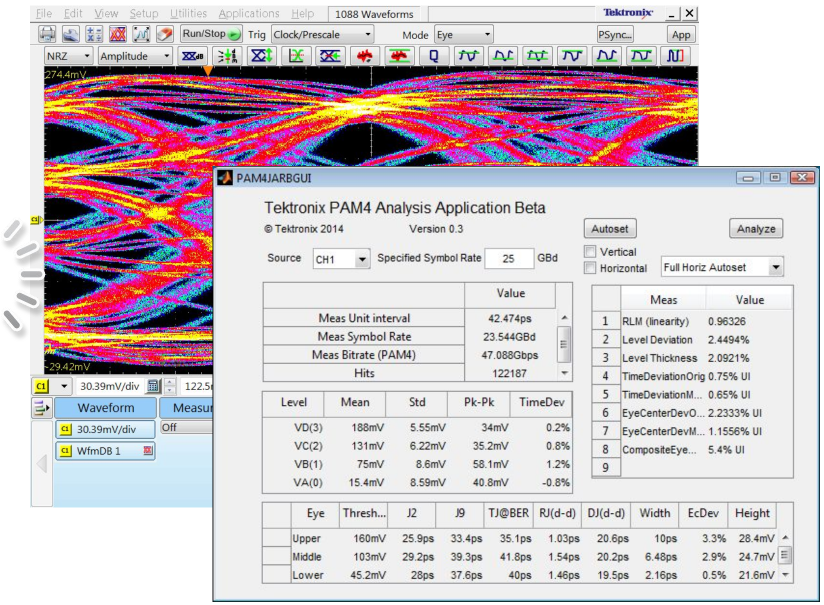
Sampling Scopes

For applications that place top priority on waveform precision

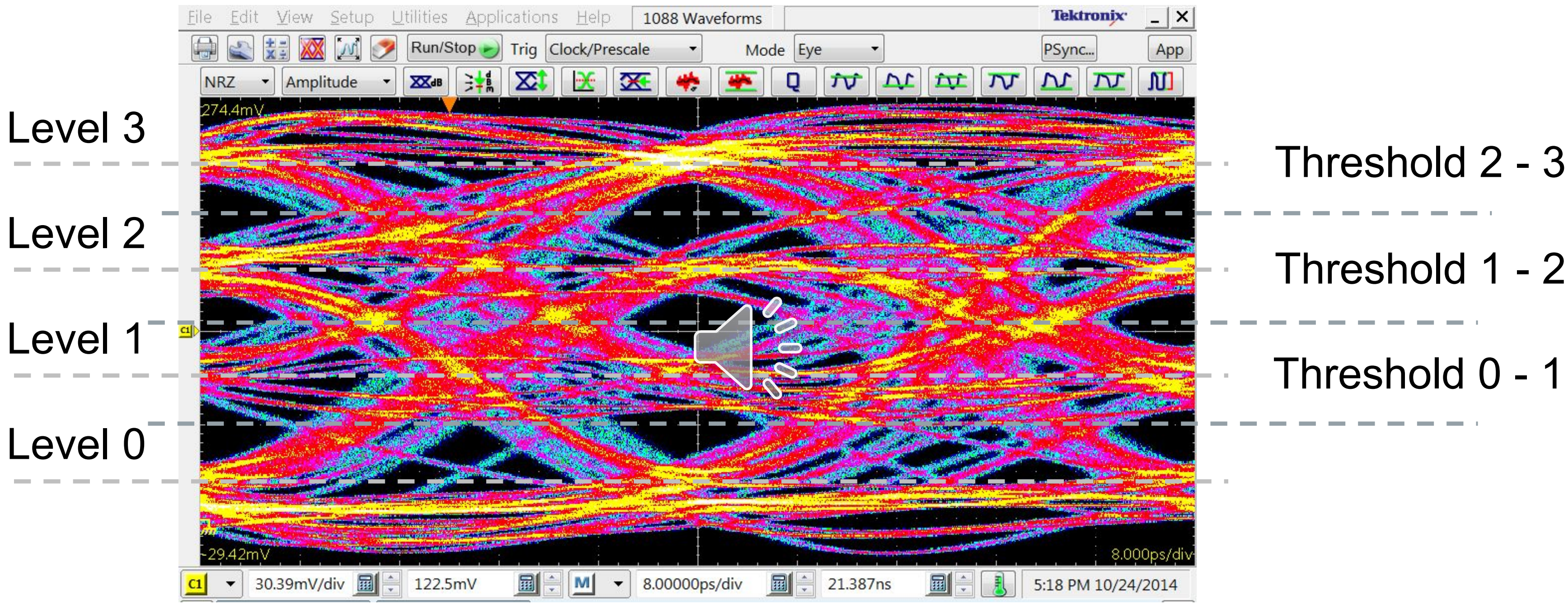
- ✓ Over 60dB of dynamic range, ideal for PAM
- ✓ High BW to 100Ghz
- ✓ Repetitive waveforms
- ✓ Very Low Jitter Noise Floor

PAM4 TX Measurements

- Inherited from 100GBASE-KP4 (PAM4 for 100 GbE backplane)
- Measurements across the entire signal
  - Level separation mismatch - R_{LM}
  - Time and Level Deviation
  - Level Thickness
  - Eye Center Deviations
  - Composite Eye Width
- Individual Eye Measurements
  - Jitter
  - Noise
  - Eye Height
  - Eye Width
- Future direction: Linear Fit, SNR overall via ‘COM’ (Channel Operational Margin), and Mask test are also being considered



TX Measurements
PAM4 Levels and Thresholds



Levels are used for determining the thresholds, calculating noise, linearity, time deviation

Thresholds are used to calculate jitter, eye centers and other eye parameters

TX Measurements
Linearity Measurement

- Measures how evenly the four signal levels are distributed
- Measured using the Linearity Pattern
- 802.3bj requires $R_{LM} > 0.92$
- Measurement made on bits 7 and 8 on each level

IEEE P802.3bj/D3.2
11th April 2014

Draft Amendment to IEEE Std 802.3-2012

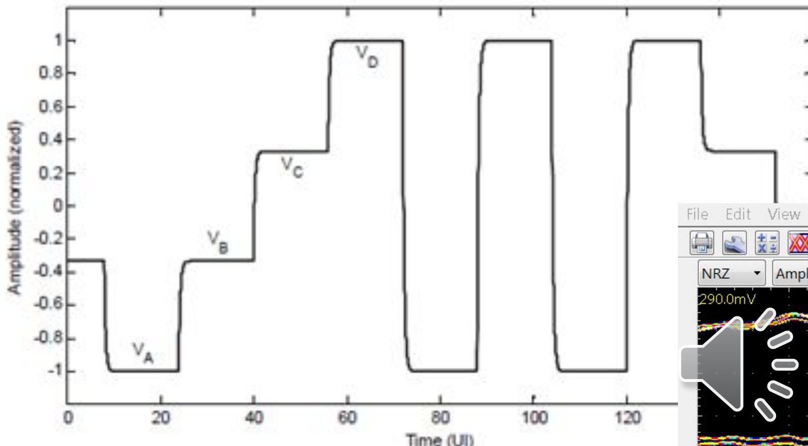


Figure 94–18—Transmitter linearity test pattern

The level separation mismatch ratio shall be greater than 0.92.

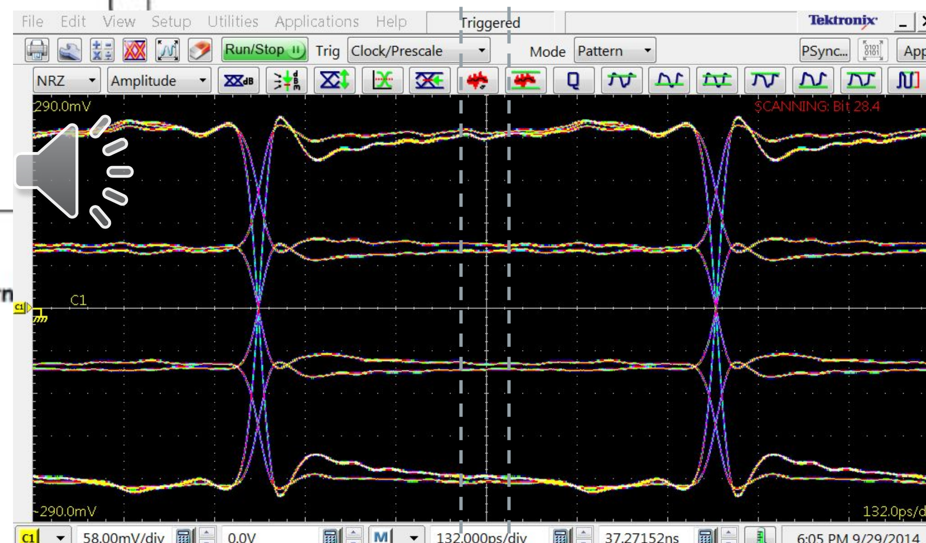
$$S_{min} = \frac{min(V_D - V_C, V_C - V_B, V_B - V_A)}{2}$$

$$V_{avg} = \frac{V_A + V_B + V_C + V_D}{4}$$

$$ES_1 = \frac{V_B - V_{avg}}{V_A - V_{avg}} \quad (94\text{–}11)$$

$$ES_2 = \frac{V_C - V_{avg}}{V_D - V_{avg}} \quad (94\text{–}12)$$

$$R_{LM} = \frac{6 \cdot S_{min}}{V_D - V_A} \quad (94\text{–}13)$$



Linearity estimate can be calculated for arbitrary pattern at the center of the UI (averaged ISI effects are included)

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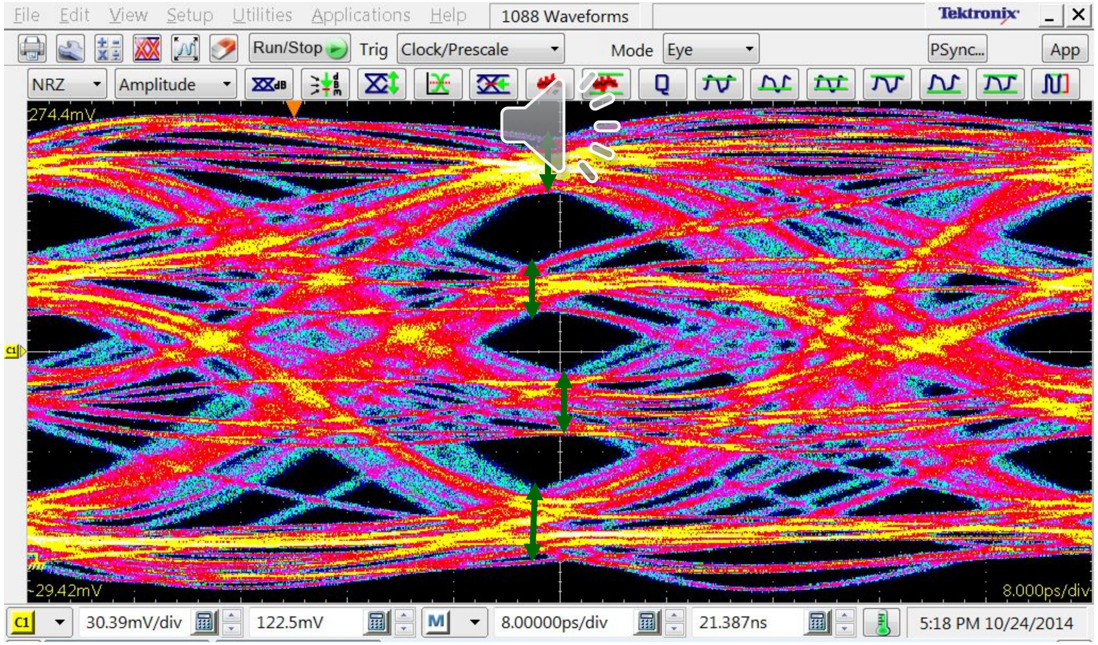
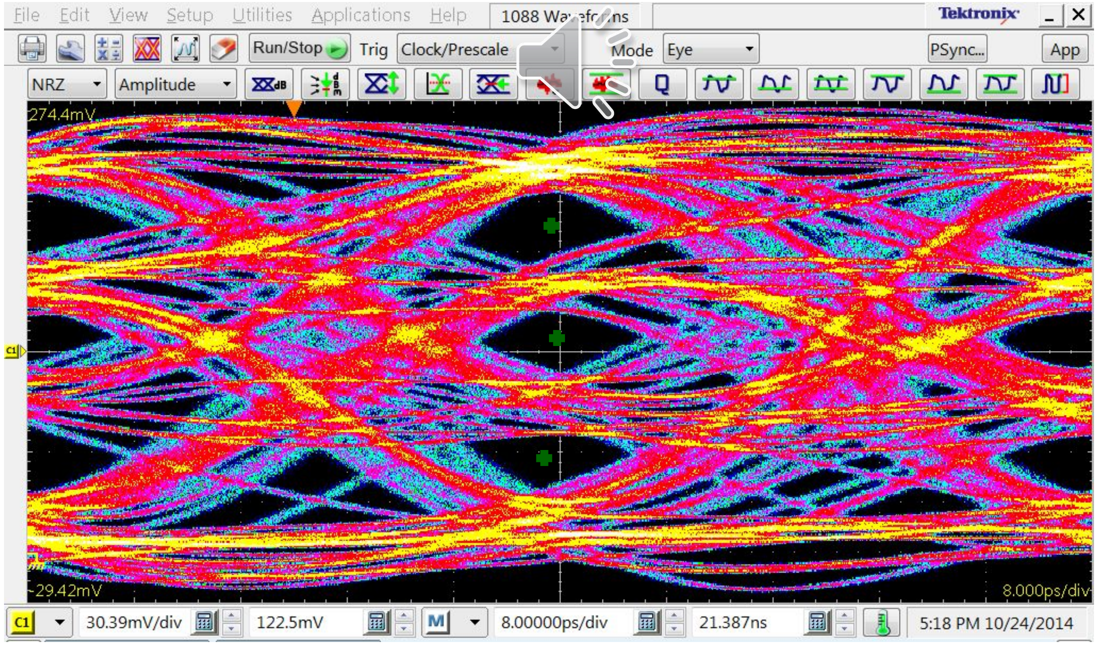
TX Measurements
Time and Level Deviation

- Characterizes timing properties of the signal and non-linear artifacts in the driver
- Looks at the skew between the narrowest point on each level
- Done on QPRBS13 pattern



TX Measurements
Eye Center Deviation

- Measures the level and time deviations in the context of the RX
- Measures linearity in terms of eye center
- Looks at the center of each eye and compares the center points
- Done on QPRBS13 pattern



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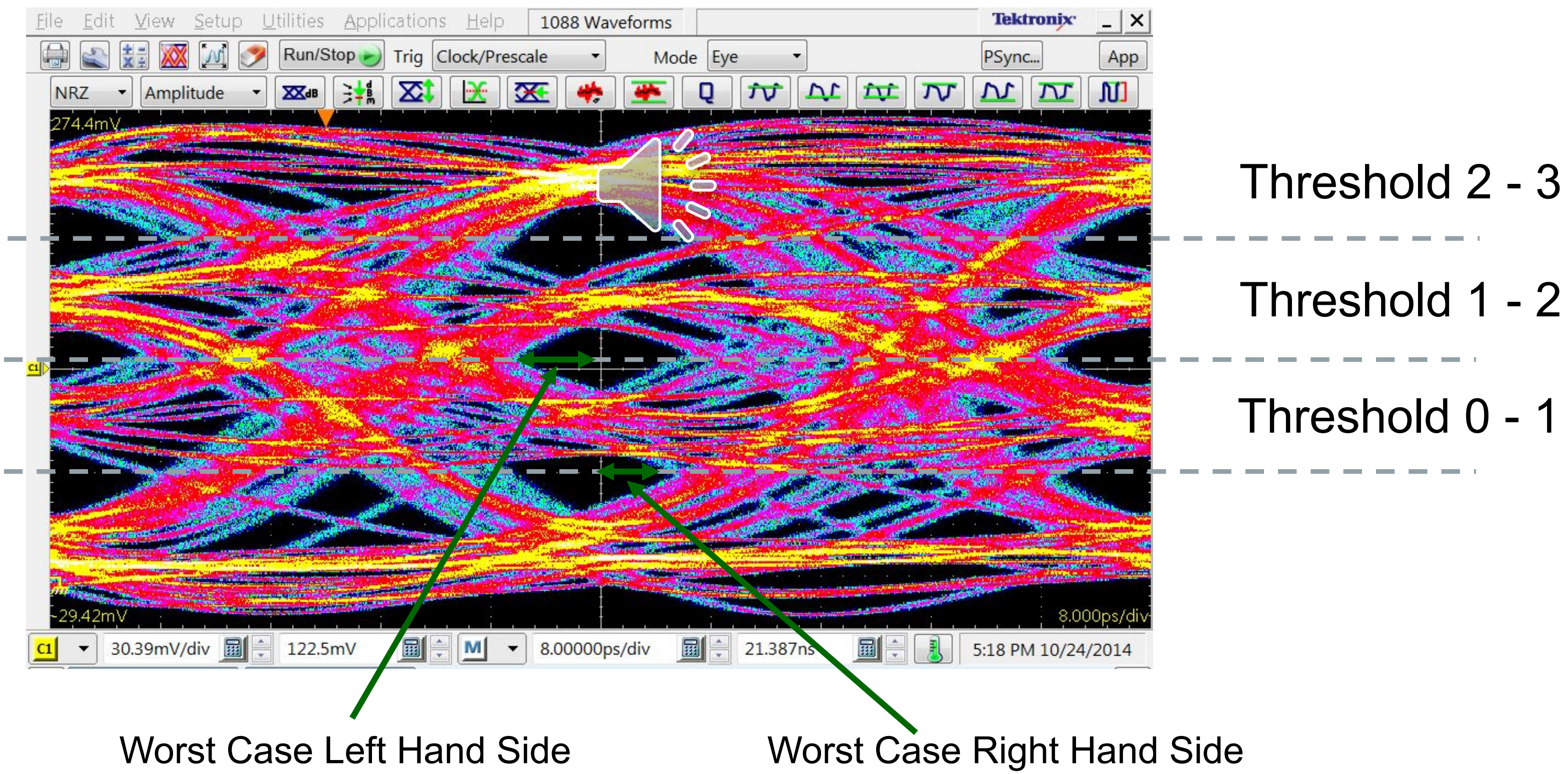
TX Measurements
Composite Eye Width

- Determines the worse case on the left and right of the slicer
- Result is the Composite Eye Width



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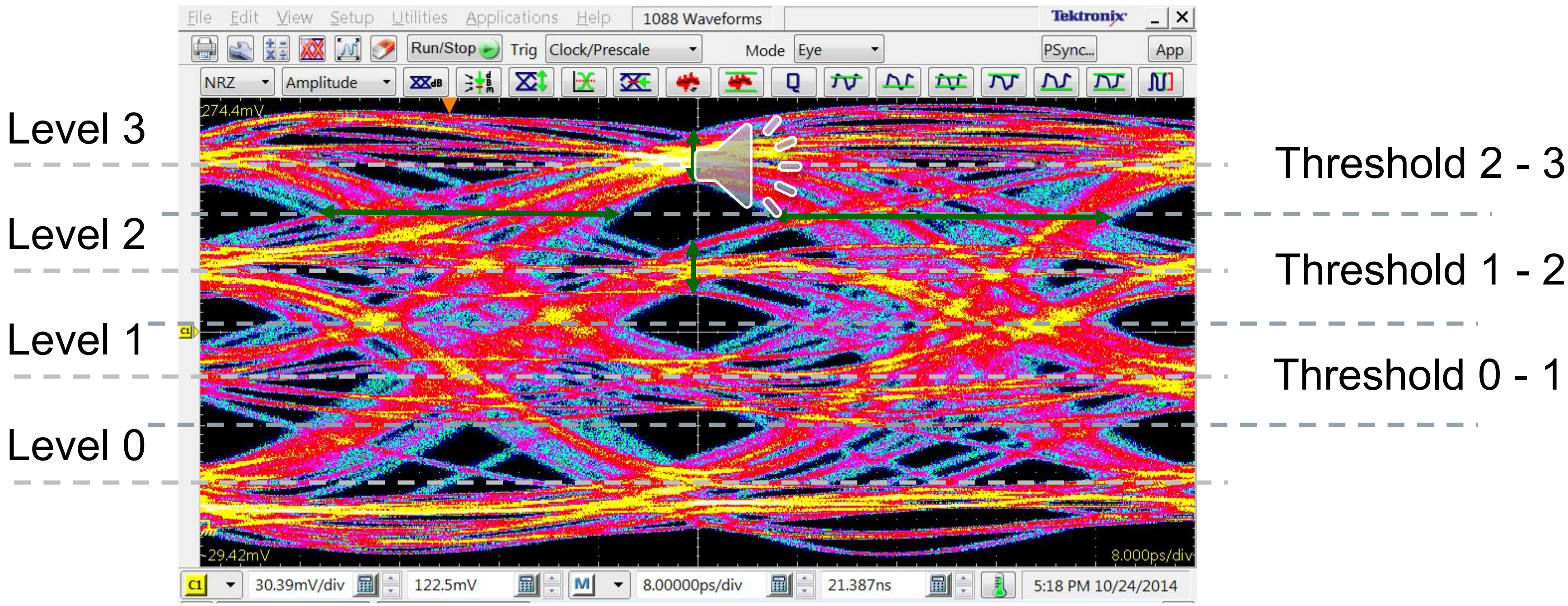
TX Measurements
Jitter and Noise

- Jitter and Noise are measured independently on each eye
- Key is to accurately determine the threshold for making the jitter measurements and level for noise measurements



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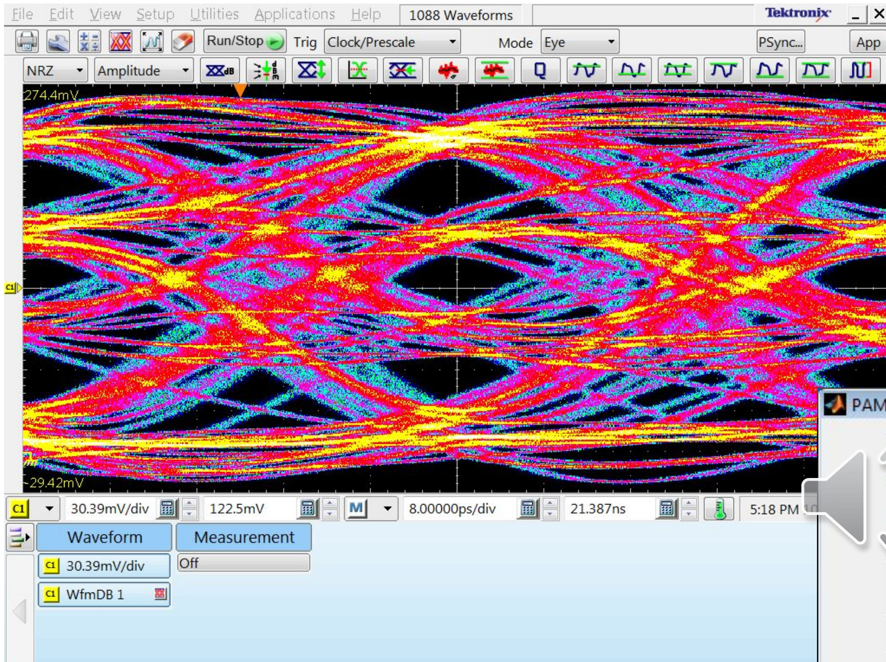
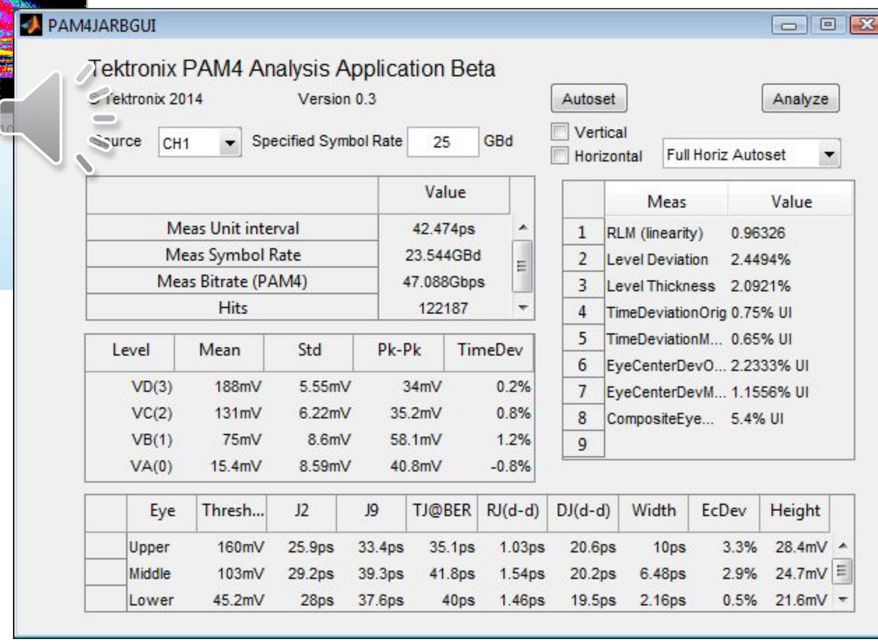
Tektronix PAM TX Analysis Solution

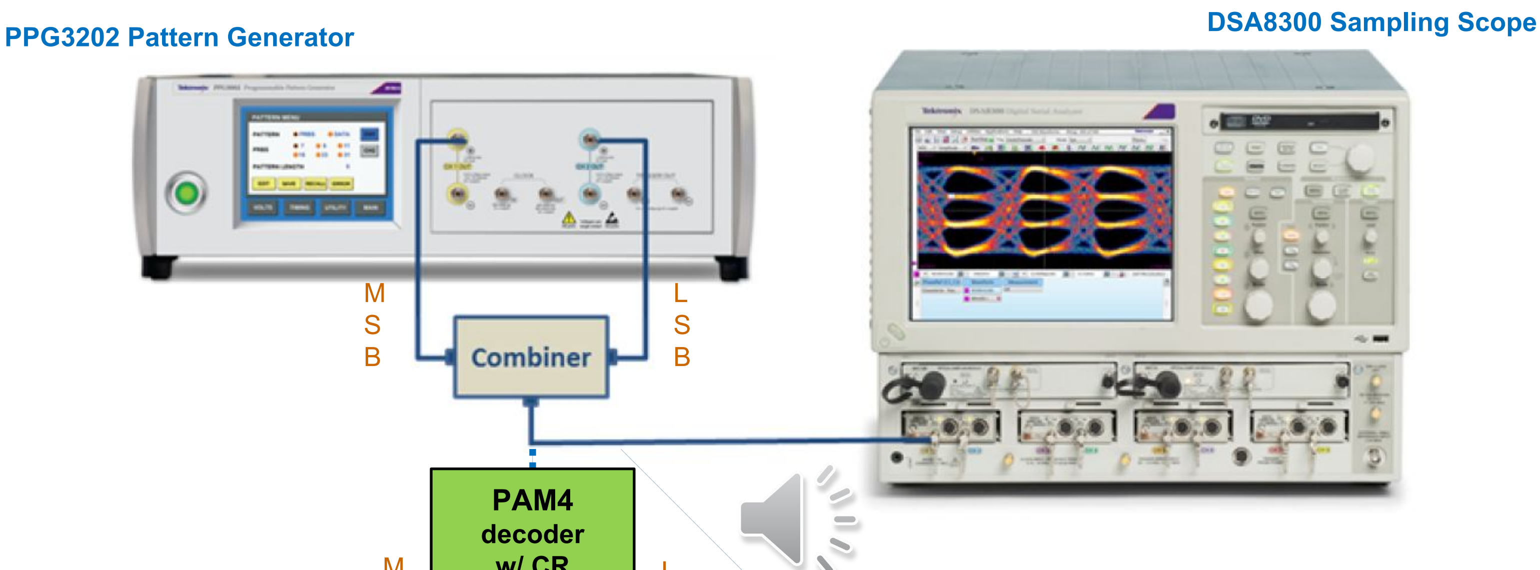


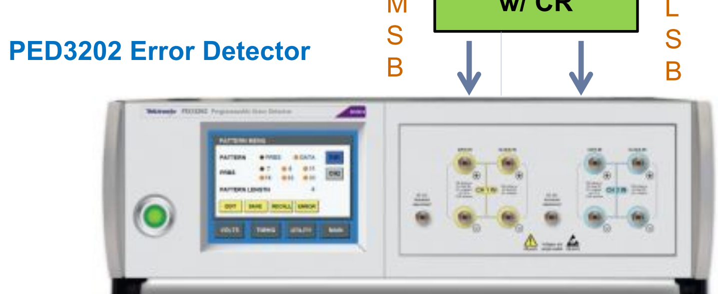
- DSA8300 Sampling Oscilloscope
  - Software Opt. JNB02 and ADVTRIG
  - 80E09B 60 GHz Electrical Sampling Module
  - 82A04B Phase Reference Module
  - Optical I/O - add one of the following:
    - 80C14 for Multi-mode PAM to 16 Gbps
    - 80C15 for Multi-mode PAM to 28 Gbps
    - 80C10C for Single mode PAM



- Available Measurements
  - Level separation mismatch - R_{LM}
  - Time and Level Deviation
  - Level Thickness
  - Eye Center Deviations
  - Composite Eye Width
  - Jitter
  - Eye Height and Width

PAM4 Generation & BER Analysis using Pattern Generators



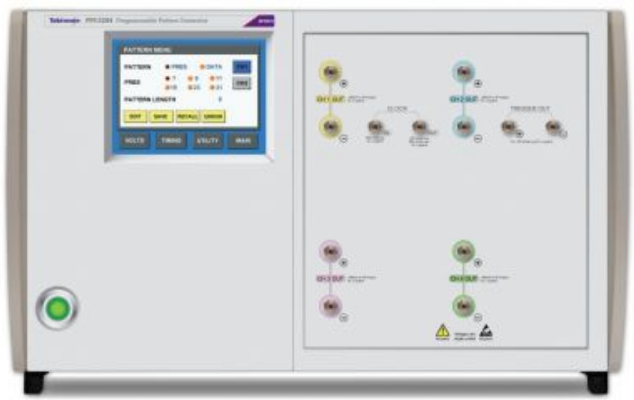


- PAM4 Pattern Generator
  - Phase-aligned channels simplify multi-level signal generation
  - User-programmable data patterns allow test of PAM4 custom data
- PAM4 Error Detector
  - BER measurements analyzes every bit of each pattern
  - Contour plots, bathtub curves, total jitter analysis via software tools
  - Can be used for BER measurements generated by PPG and/or AWG

- BERT products bundled into a PAM4 system:
  - Programmable pattern generator
  - Programmable error detector
  - Analysis software
  - Broadband components (power combiners/attenuators)

High Performance Instruments

High Quality Analog Inputs and Outputs



Pattern Generators

- **12.5G**, **16G, 30G**, **32G**, and **40G** Models
- Fast risetime
- Low jitter
- Multi-channel
- NRZ and PAM-4
- Jitter insertion
- Pre-emphasis
- Front panel and remote control

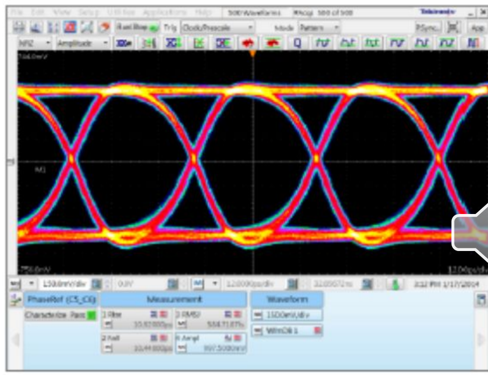
Error Detectors

- **32G** and **40G** Models
- High sensitivity
- Wide phase margin
- Multi-channel
- NRZ and PAM-4
- Auto sync and phase align
- Bathtub and contour analysis
- Front panel and remote control

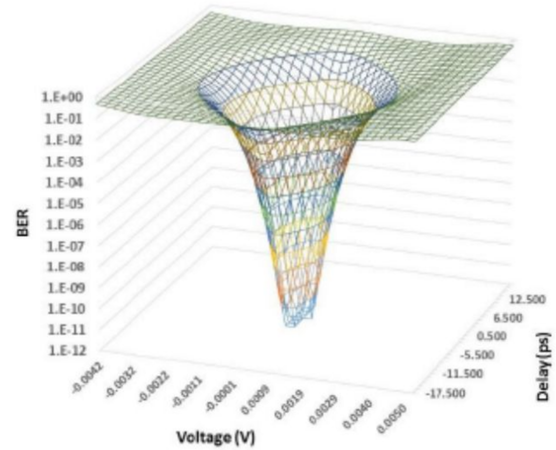
Improvements Result in
Industry Best Performance!

Best in Class BERT Performance

Picosecond Pulse Labs, Boulder, CO 80301



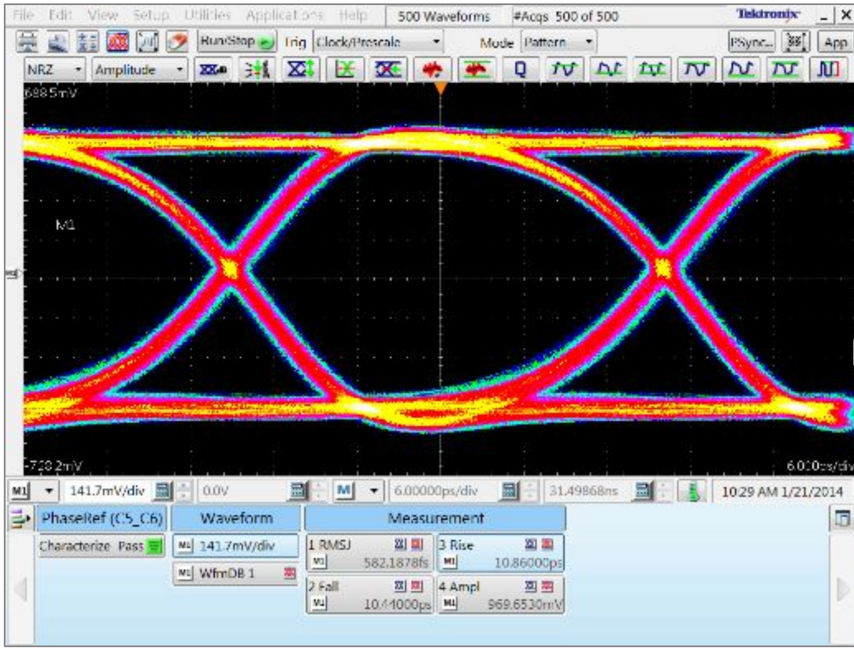
Lowest Pattern Generator 32 Gb/s Jitter in the Industry with 7.5 ps TJ (1e-12) and 250 fs RJ [1,2]



Highest Sensitivity Error Detector in the Industry with <6 mVpp at 28.1 Gb/s [1,3]

Picosecond Pulse Labs' **PatternPro**™ serial data instruments have recently been improved to provide the **highest performance of any BERT instruments in their class**. Today's high-speed test applications demand the best performance possible and the key performance parameters are pattern generator inherent jitter and error detector sensitivity. This applications brief gives details of the measured jitter and sensitivity for the Model 12072 32 Gb/s pattern generator and the Model 13025 32 Gb/s error detector.

Fast Risetime and Low Jitter
32Gb/s Multi-channel PPG



PPG320X 32Gb/s
OPT-ADJ

Data Source: MATH1 SSC: Off Phase Reference: 32 GHz	Data Rate: 32 Gbps Pattern: 2047 bits Sample Count: 304.70 k	Filter: False Channel: False Equalizer: None

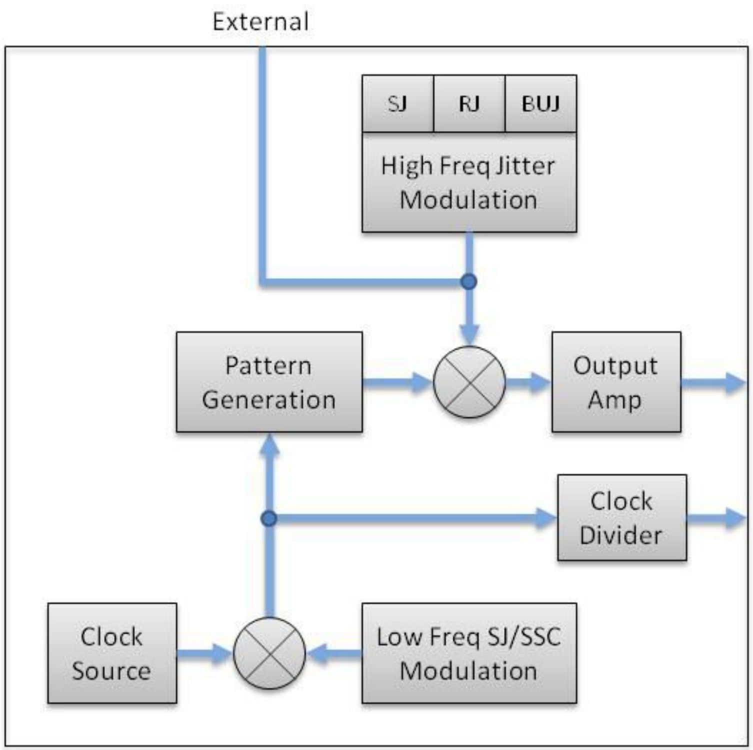
Jitter (Decision Threshold: -11.95 mV)		
Random Jitter		
RJ (RMS)	=	211.36 fs
RJ(h) (RMS)	=	21[illegible].20 fs
RJ(v) (RMS)	=	8.[illegible]9 fs
Deterministic Jitter		
DJ	=	[illegible].94 ps
DDJ	=	3.20 ps
DCD	=	971.00 fs
DDPWS	=	2.77 ps
BUJ(d-d)	=	50.00 fs
PJ	=	718.02 fs
PJ(h)	=	717.99 fs
PJ(v)	=	6.79 fs
NPJ(d-d)	=	50.00 fs
Total Jitter @ BER		
TJ (1E-12)	=	6.76 ps
Eye Opening (1E-12)	=	2[illegible].49 ps
Dual Dirac		
RJ(d-d)	=	243.96 fs
DJ(d-d)	=	3.32 ps

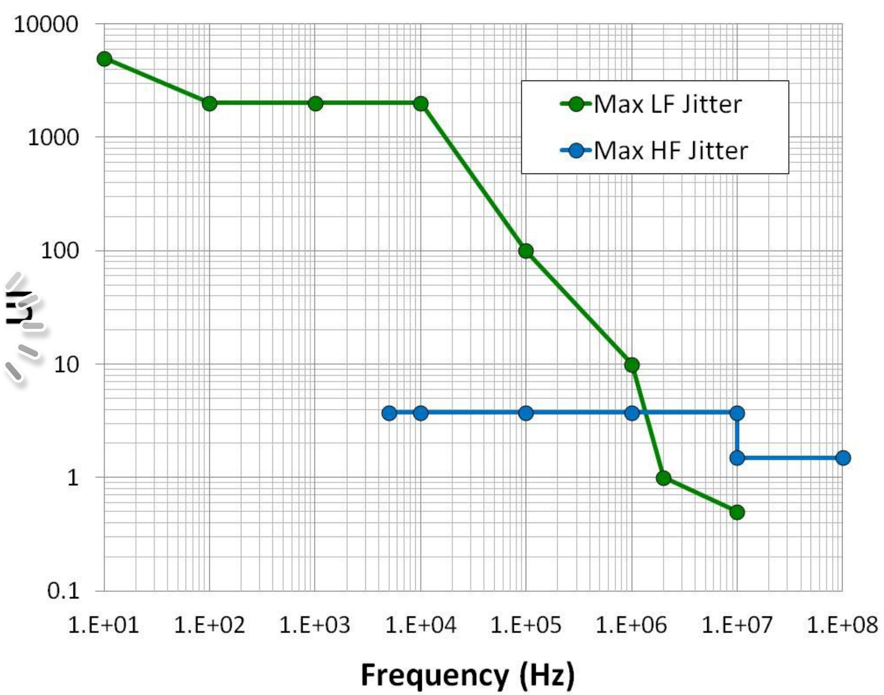
Noise (Sampling Phase: 0 UI)		
Random Noise		
RN (RMS)	=	581.45 uV
RN(v) (RMS)	=	567.11 uV
RN(h) (RMS)	=	128.35 uV
Deterministic Noise		
DN	=	149.69 mV
DDN	=	149.22 mV
DDN(level 1)	=	124.94 mV
DDN(level 0)	=	167.15 mV
BUN(d-d)	=	1.74 mV
PN	=	633.25 uV
PN(v)	=	458.95 uV
PN(h)	=	436.33 uV
NPN(d-d)	=	1.70 mV
Total Noise @ BER		
TN (1E-12)	=	157.72 mV
Eye Opening (1E-12)	=	821.79 mV
Eye Amplitude	=	979.51 mV
SSC Modulation		
Magnitude	=	0 ppm
Frequency	=	0 Hz

Industry Best 32Gb/s
Jitter Performance!
Rj=211fs

DSA8300
80E11 sampling plug-in
82A04-60G phase reference

Jitter Insertion Architecture and Ranges



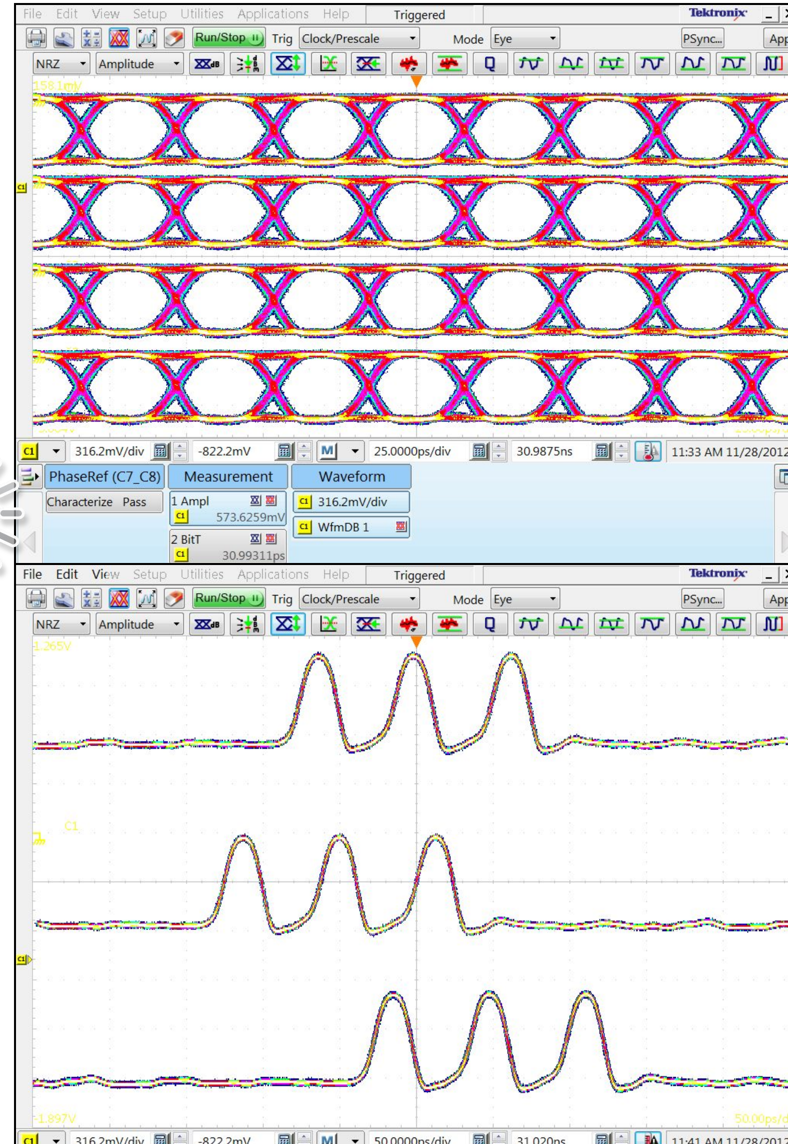


OPT-LFJ with OPT-HFJ ranges.
Based on 25Gb/s data rate.

Bit-aligned multi channel output

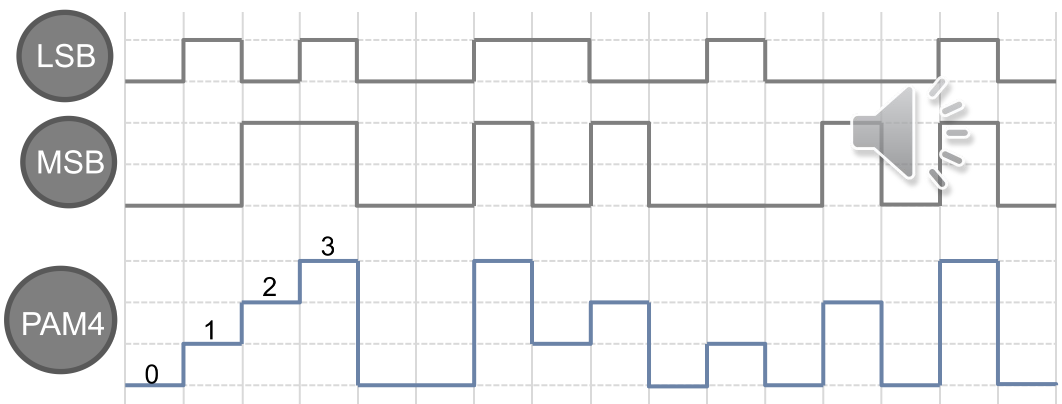
PPG3204 output with aligned bits

+/- 50 pS channel-to-channel skew adjustment capability



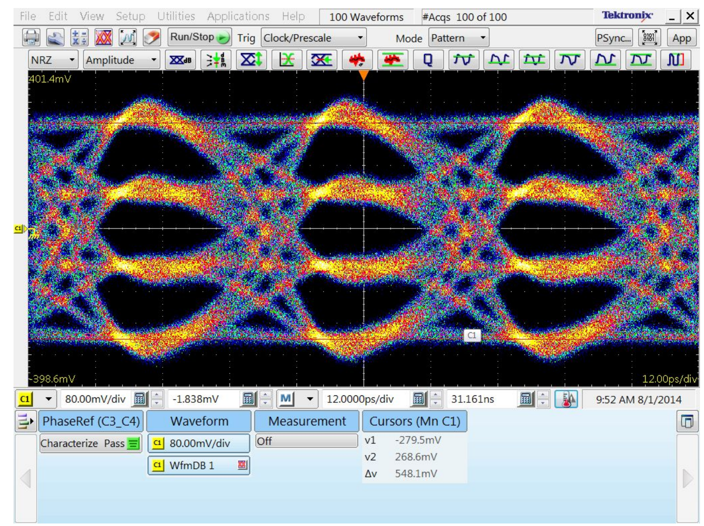
PAM4 Signal Generation with PPG

- Ultra-high quality signal with fast risetimes and low inherent jitter
- Uses two channel PPG to set up PAM4 signal
  - Uses external combiner kit (PSPL5350) to combine two phase-aligned channels
  - Phase-aligned channels simplify multi-level signal generation
  - User-programmable data patterns allow test of PAM4 custom data
- Program same PRBS with LSB-MSB bit shift or program different user-defined patterns with the same length on PPG channels.



LSB: Ch1 data signal (1V)
MSB: Ch2 data signal (2V)
PAM4: Sum of the two signals

MSB	LSB	PAM4 LEVEL
0	0	0
0	1	1
1	0	2
1	1	3



56Gbps PAM4 Signal

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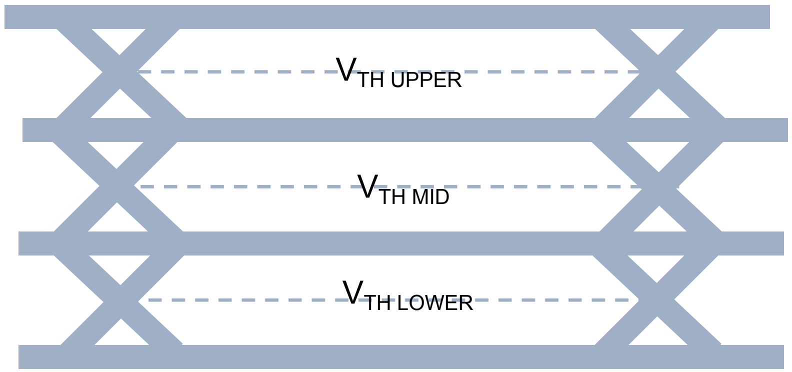
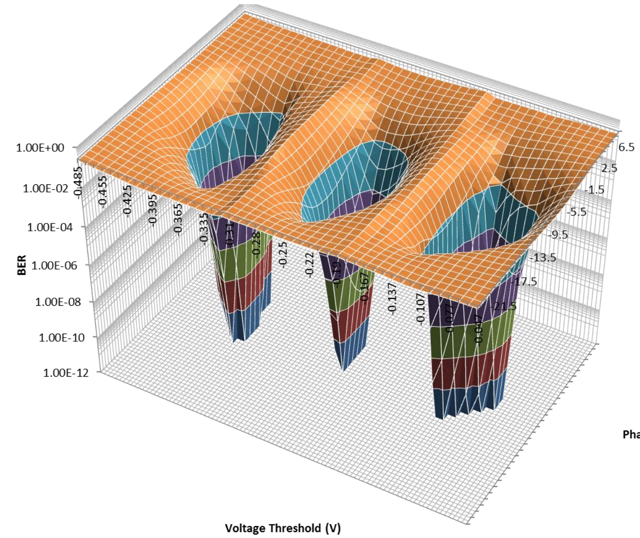
PAM4 Error Detection and Analysis





- Define three PED patterns using the following criteria:
  - "lower eye" equals 'OR" of LSB with MSB
  - "middle eye" equals MSB
  - "upper eye" equals "AND" of LSB with MSB
- Use PED and PC GUI software to test all three PAM4 eye diagrams
  - **BER measurements** analyzes every bit of each pattern
  - Automatic alignment and pattern synchronization
  - Contour plots, bathtub curves, total jitter **analysis** via software tools
  - **6mVpp PED sensitivity is the best in the industry**
- PC GUI utility provides automated procedures for these steps

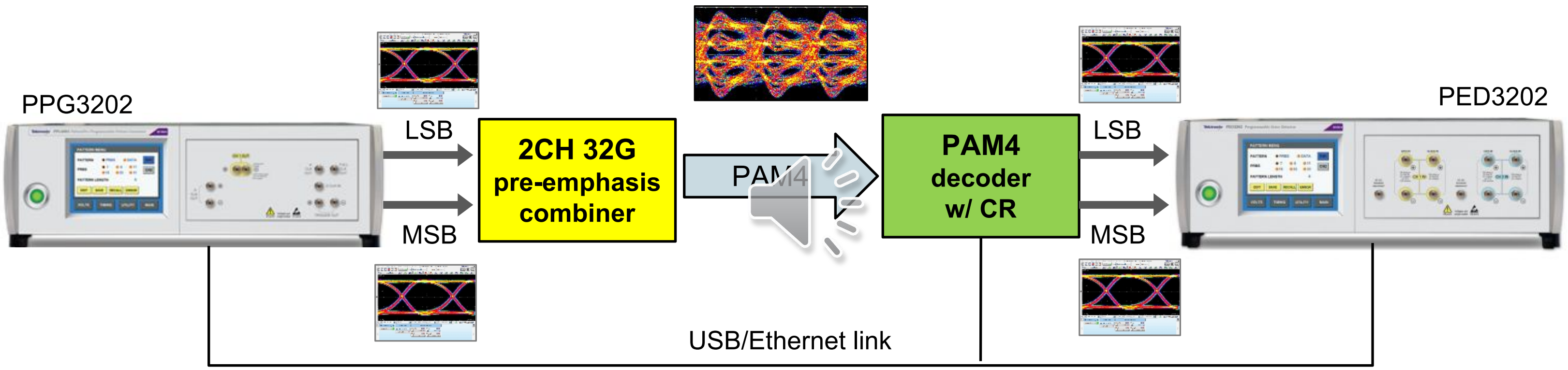
New PAM4 Test Solutions

PAM4 signal generation

- Auto-alignment of PAM4 signal (LSB/MSB)
- Programmable **Tx pre-emphasis** for channel compensation
- Independent programming of LSB and MSB data
- **PRBS31** and user data patterns

PAM4 signal analysis

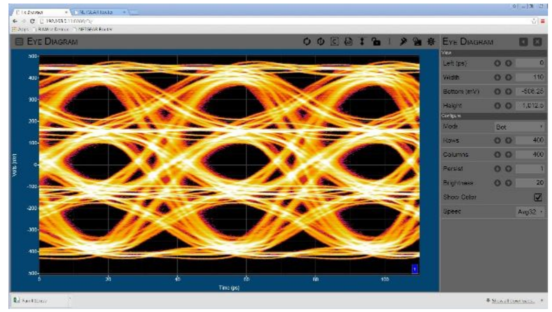
- Auto-alignment of PAM4 signal at decoder
- Integrated **clock recovery**
- **True BER** measurement of all LSB and MSB data
- **PRBS31** and user data patterns

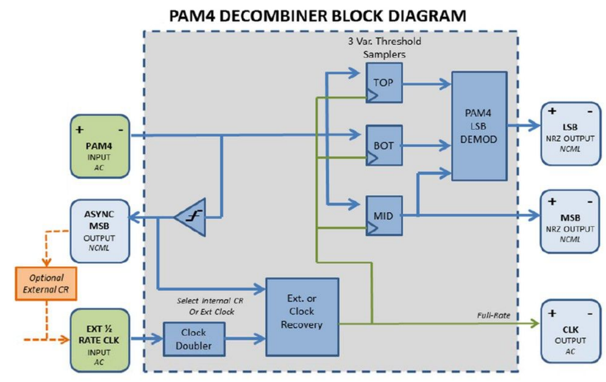


PAM4 control software

- **Full GUI** with PAM4 eye display at decoder input
- Signal generation and analysis control from a single software console
- **Automated routines** for Tx alignment and Rx analysis

PAM4 Decoder

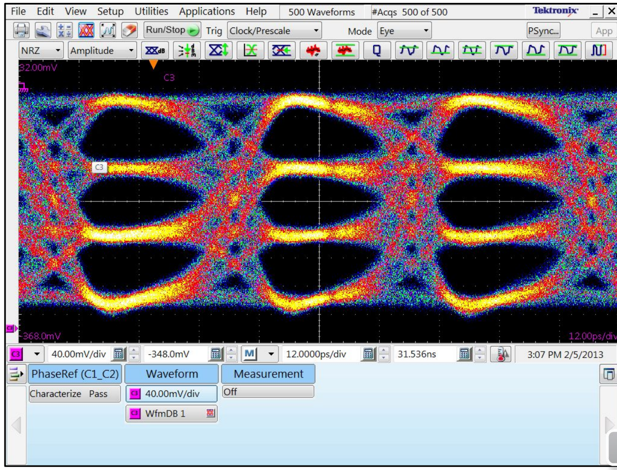


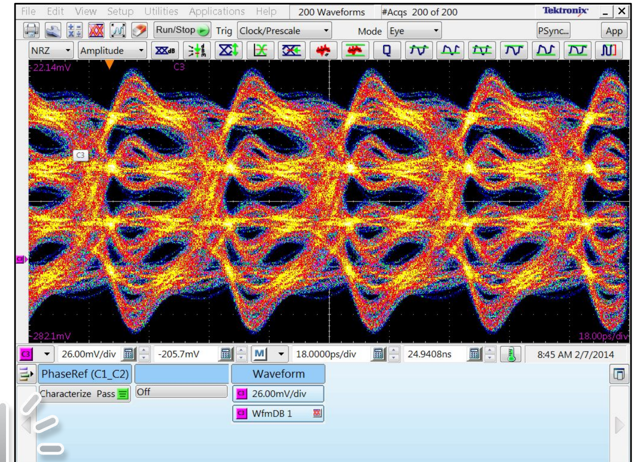


- PAM4 Decoder Box available for demo April 2015
  - Full true PAM4 BER test with PPG and PED instruments
  - Integrated PAM4 PED solution under investigation
- Operates with recovered or external clock in
- Includes GUI interface for PAM4 Tx alignment and eye monitoring
- Aligns clock to data and selects vertical/horizontal sampling points

PAM4 Pre-emphasized signal

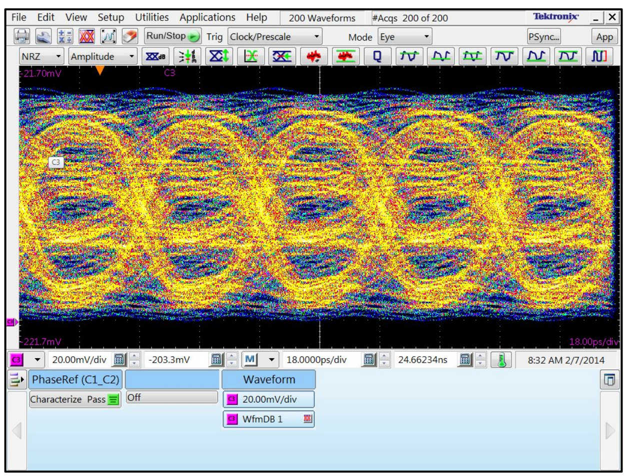
Standard PAM4

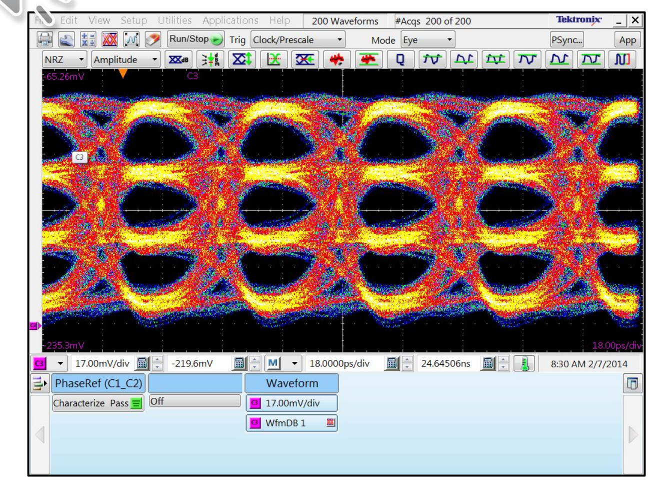




Emphasized PAM4

Standard PAM4 w/ 6' Cable

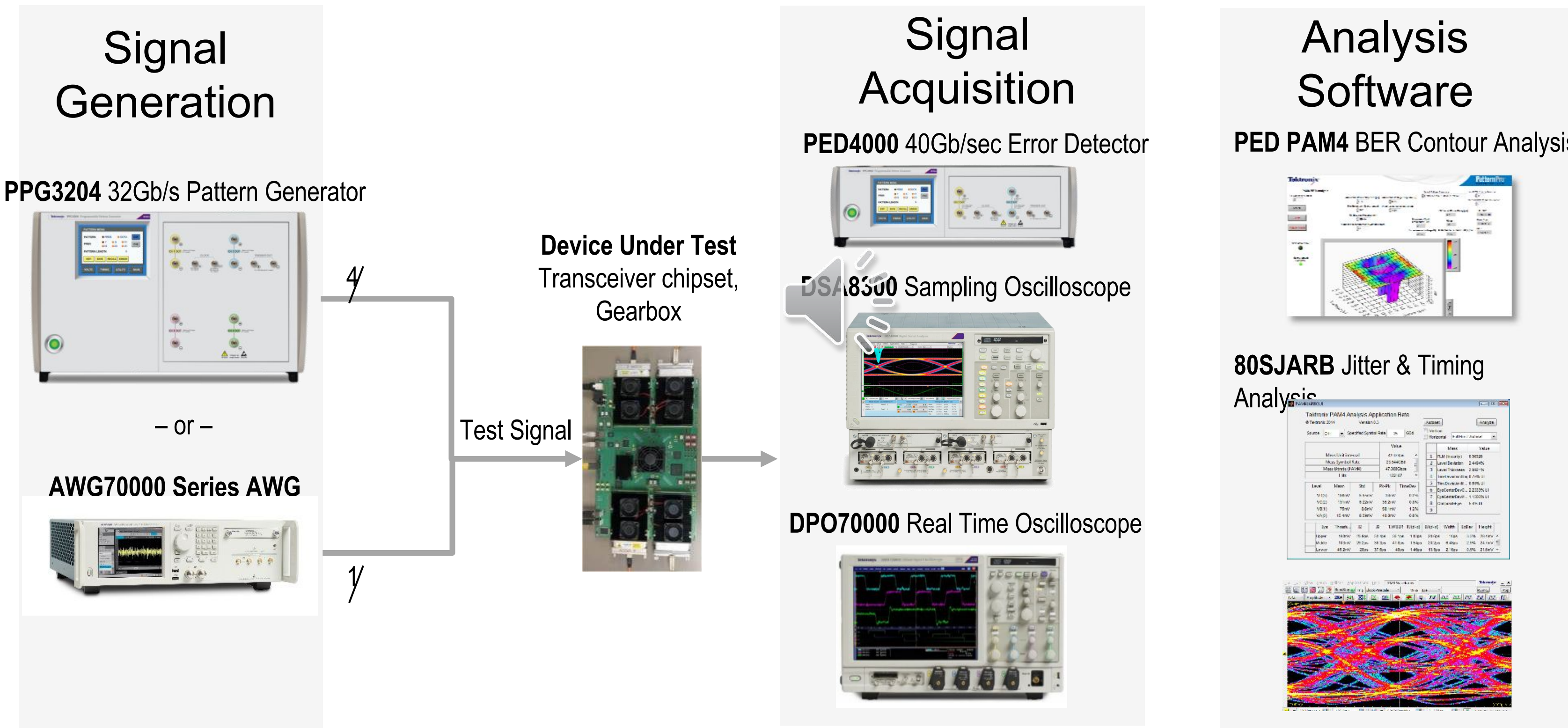




Emphasized PAM4 w/ 6' Cable

Test Methodologies for PAM Signaling Validation

Tektronix provides complete support for validation of PAM4 at 28 & 56G



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Summary / Q&A

- For more information, please visit www.tek.com/100G